AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for programming a plurality of magnetic memory cells, the plurality of magnetic memory cells being coupled to a bit line, the plurality of magnetic memory cells being associated with a plurality of digit lines, the method comprising the steps of:

(a) providing a predetermined bit line current I_B in the bit line at a predetermined bit line voltage V_B; and

(b) providing a plurality of predetermined digit currents I_D in parallel in the plurality of digit lines at a predetermined digit line voltage V_D for the plurality of magnetic memory cells at substantially the same time as the bit line current I_B, the plurality of digit currents and the bit line current allowing the plurality of magnetic memory cells to be written to a plurality of states in parallel, wherein the total power supplied to the plurality of magnetic memory cells during writing is $I_BV_B + NI_DV_D$, where N is the number of digit lines.

2. (Original) The method of claim 1 wherein the bit line current is applied for a first predetermined time and the plurality of digit currents is provided for a second predetermined time.

3. (Original) The method of claim 2 wherein the first predetermined time is two nanoseconds.

4. (Original) The method of claim 3 wherein the second predetermined time is 1.6 nanoseconds.

PAGE 5/9 * RCVD AT 3/20/2006 5:26:08 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/4 * DNIS:2738300 * CSID:949 672 6626 * DURATION (mm-ss):04-10

5. (Currently Amended) A magnetic memory comprising:

a plurality of magnetic memory cells

a bit line, the plurality of magnetic memory cells being coupled to the bit line;

a plurality of digit lines, the plurality of magnetic memory cells being associated with the plurality of digit lines;

at least one write circuit configured to provide a predetermined bit line current I_B in the bit line at a predetermined bit line voltage V_B and to provide a plurality of predetermined digit currents I_D in parallel in the plurality of digit lines at a predetermined digit line voltage V_D in parallel at substantially the same time as the bit line current I_B, the plurality of digit currents and the bit line current allowing the plurality of magnetic memory cells to be written to a plurality of states in parallel, wherein the total power supplied to the plurality of magnetic memory cells during writing is $I_BV_B + NI_DV_D$, where N is the number of digit lines.

6. (Original) The magnetic memory of claim 5 wherein the bit line current is applied for a first predetermined time and the plurality of digit currents is provided for a second predetermined time.

7. (Original) The magnetic memory of claim 6 wherein the first predetermined time is two nanoseconds.

8. (Original) The magnetic memory of claim 7 wherein the second predetermined time is 1.6 nanoseconds.

PAGE 6/9 * RCVD AT 3/20/2006 5:26:08 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/4 * DNIS:2738300 * CSID:949 672 6626 * DURATION (mm-ss):04-10